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Itano et al.

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(54) **PHOTOELECTRIC CONVERSION APPARATUS AND IMAGE PICKUP SYSTEM INCLUDING AN AD CONVERSION UNIT TO CONVERT A SIGNAL INTO A DIGITAL SIGNAL**

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H04N 5/365 (2011.01)
H04N 5/378 (2011.01)

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CPC ***H04N 5/3658*** (2013.01); ***H04N 5/378*** (2013.01)

(58) **Field of Classification Search**
CPC H04N 5/378
USPC 348/300, 301
See application file for complete search history.

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(57) **ABSTRACT**

Column signal processing units are provided in correspondence with respective columns of a pixel array. The column signal processing unit includes a sample-and-hold unit configured to hold an analog signal output from a pixel, a buffer unit configured to buffer the signal held in the sample-and-hold unit, and an AD conversion unit. The AD conversion unit converts the signal held by the sample-and-hold unit and buffered by the buffer unit into a digital signal.

17 Claims, 13 Drawing Sheets

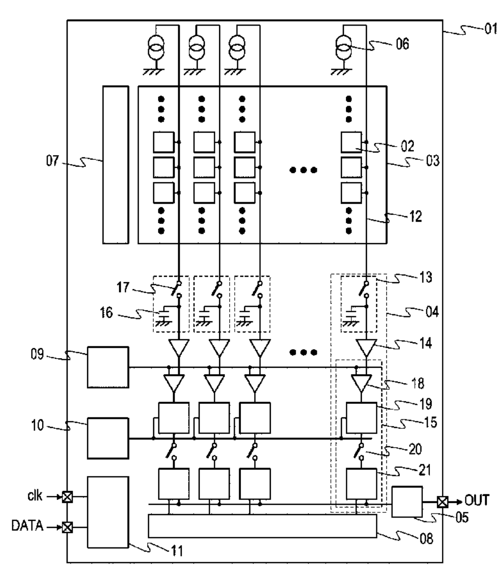
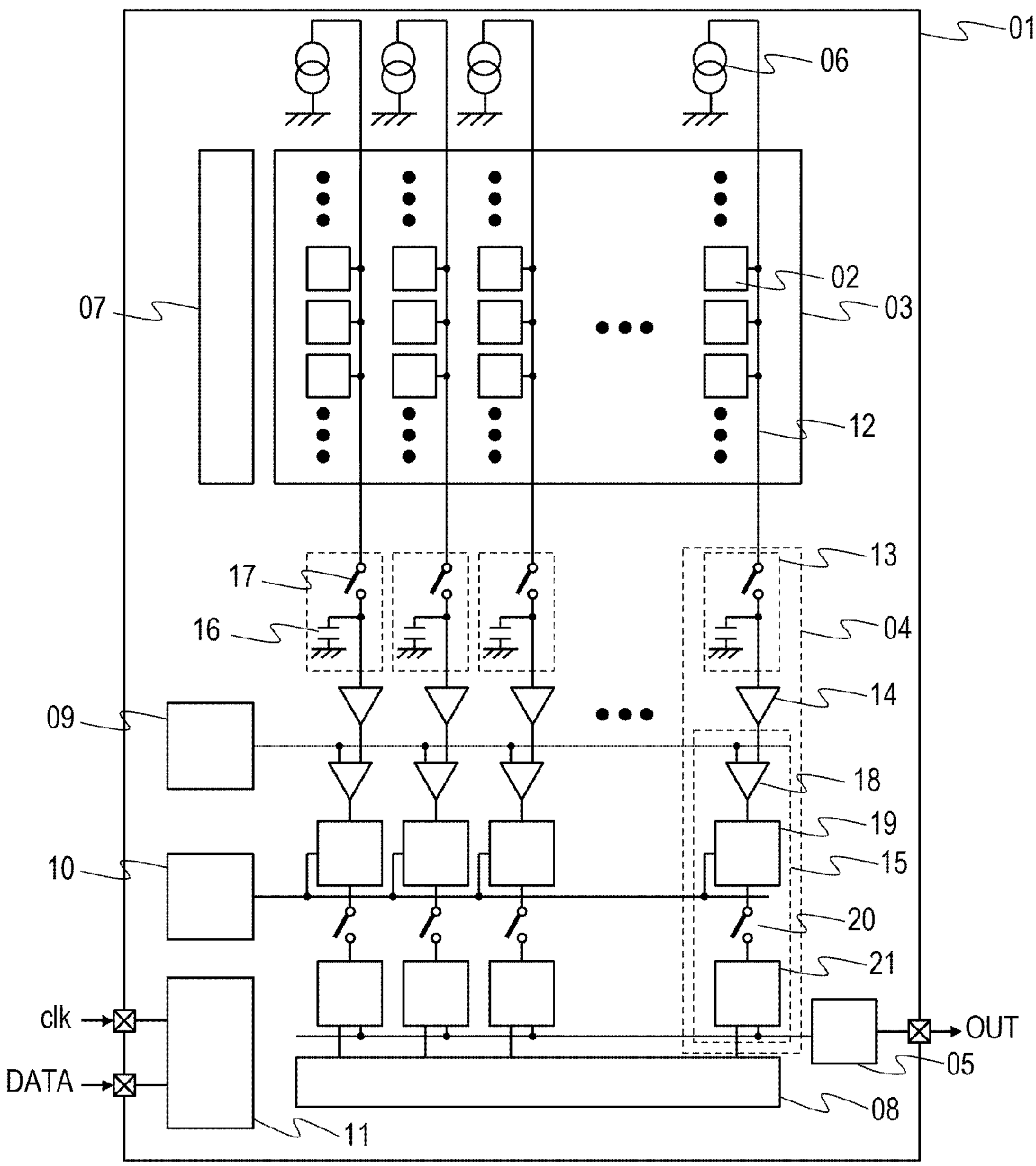


FIG. 1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06
07
02
03
12
17
13
16
04
14
09
18
19
10
15
20
21
clk
DATA
OUT
05
08
11

FIG. 2

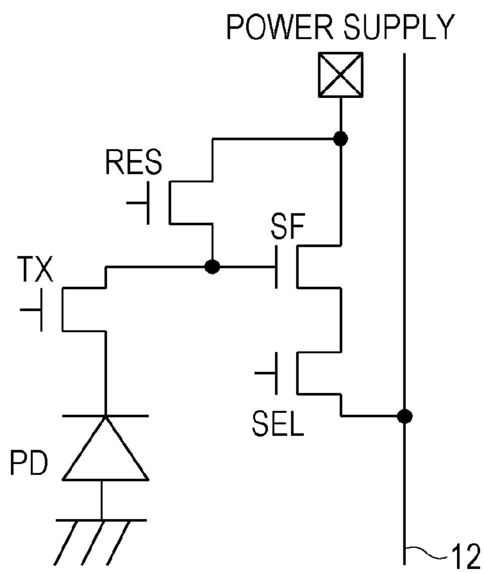


FIG. 3

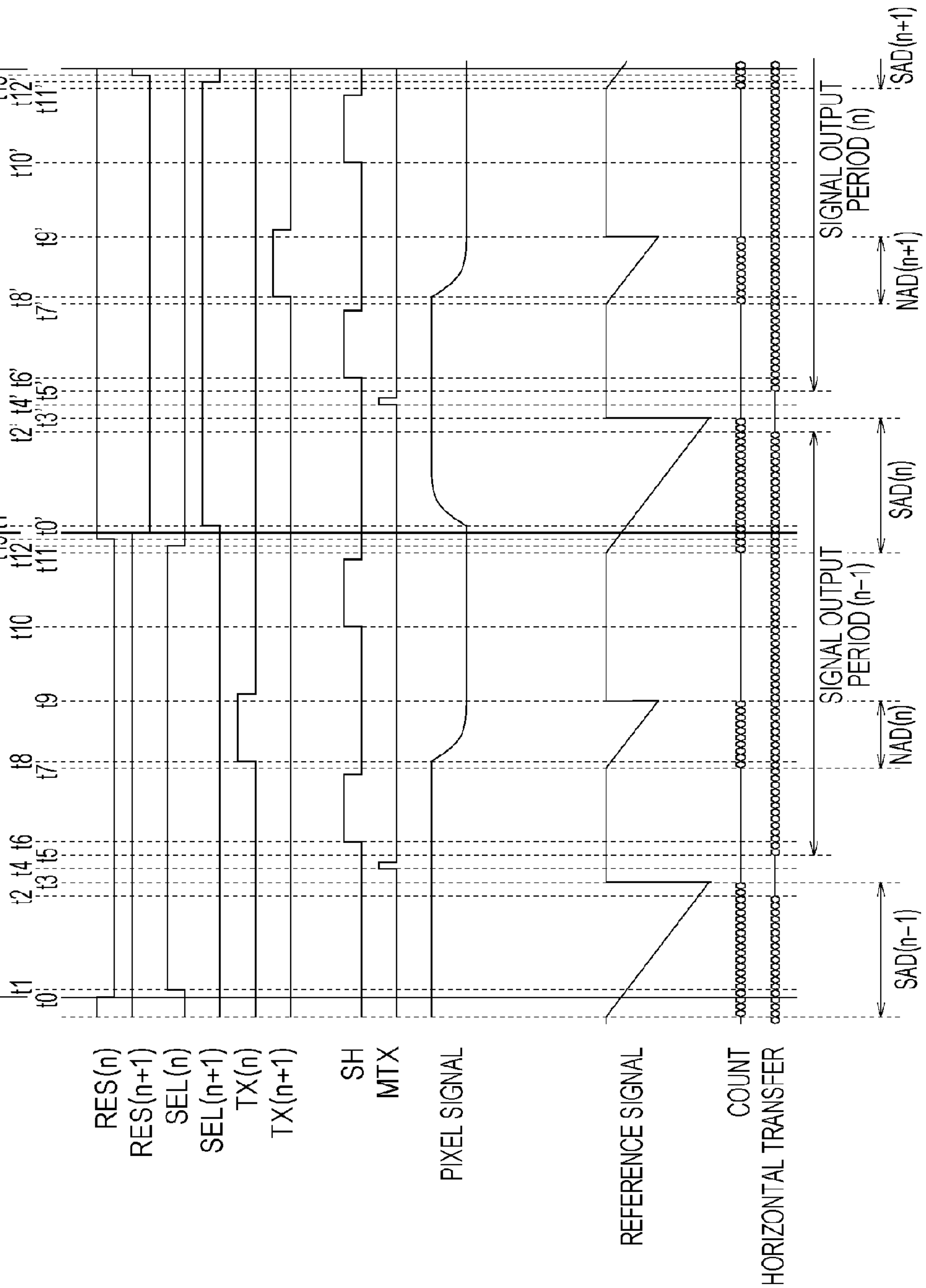

PIXEL READING PERIOD (n)
PIXEL READING PERIOD (n + 1)
t0 t1 t2 t3 t4 t5 t6 t7 t8 t9 t10 t11 t12 t13
t0' t1' t2' t3' t4' t5' t6' t7' t8' t9' t10' t11' t12' t13'
RES(n)
RES(n+1)
SEL(n)
SEL(n+1)
TX(n)
TX(n+1)
SH
MTX
PIXEL SIGNAL
REFERENCE SIGNAL
COUNT
HORIZONTAL TRANSFER
SIGNAL OUTPUT PERIOD (n−1)
SIGNAL OUTPUT PERIOD (n)
SAD(n−1)
NAD(n)
SAD(n)
NAD(n+1)
SAD(n+1)

FIG. 4

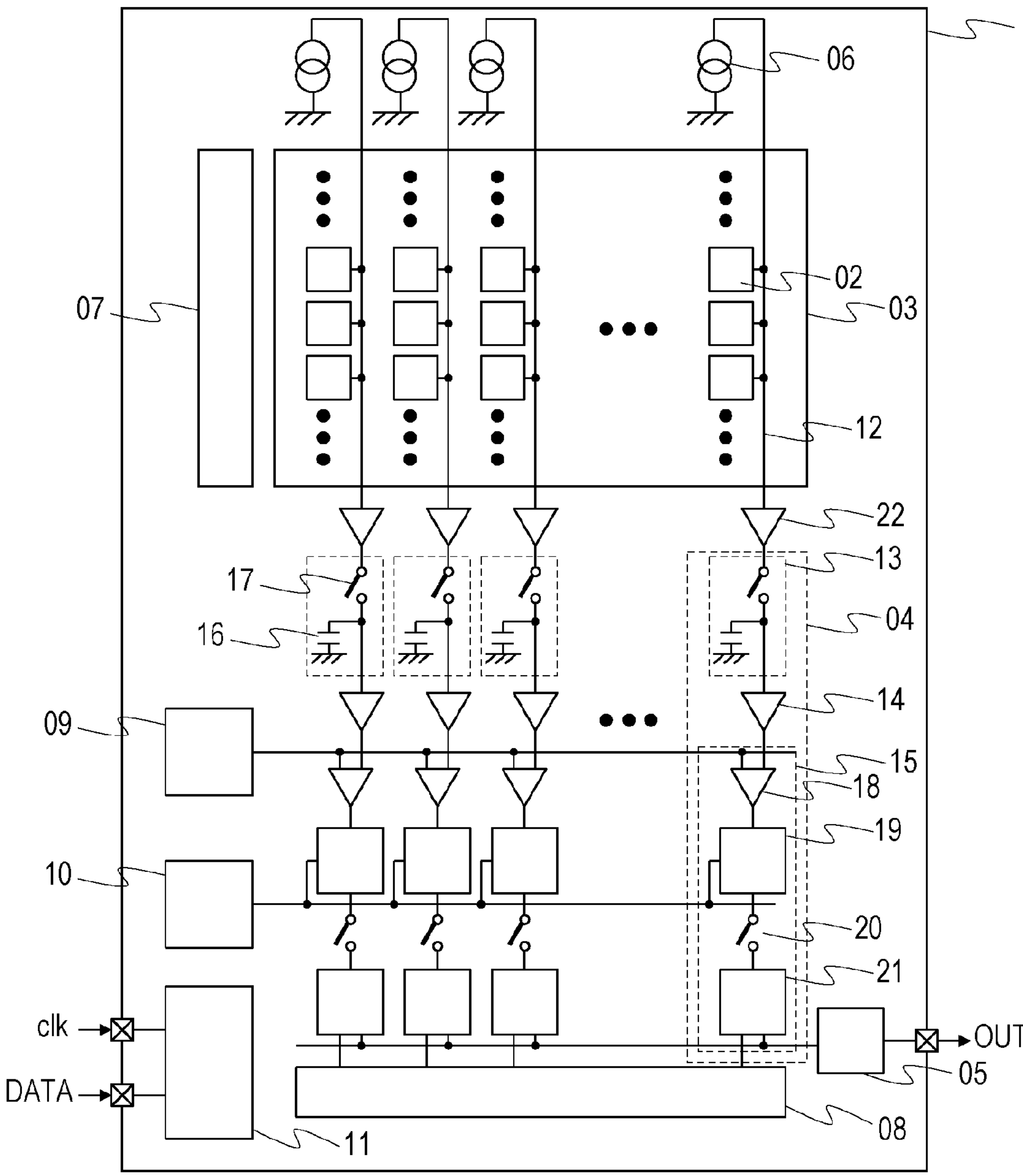

01'
06
02
03
07
12
22
13
17
04
16
14
09
15
18
19
10
20
21
clk
OUT
DATA
05
08
11

FIG. 5

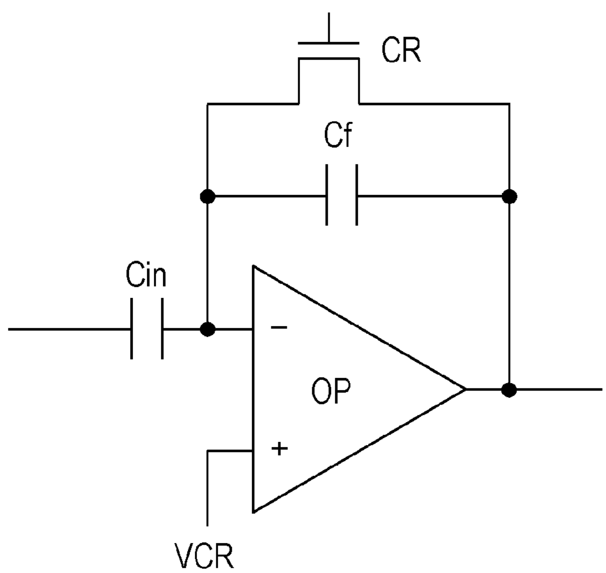


FIG. 6

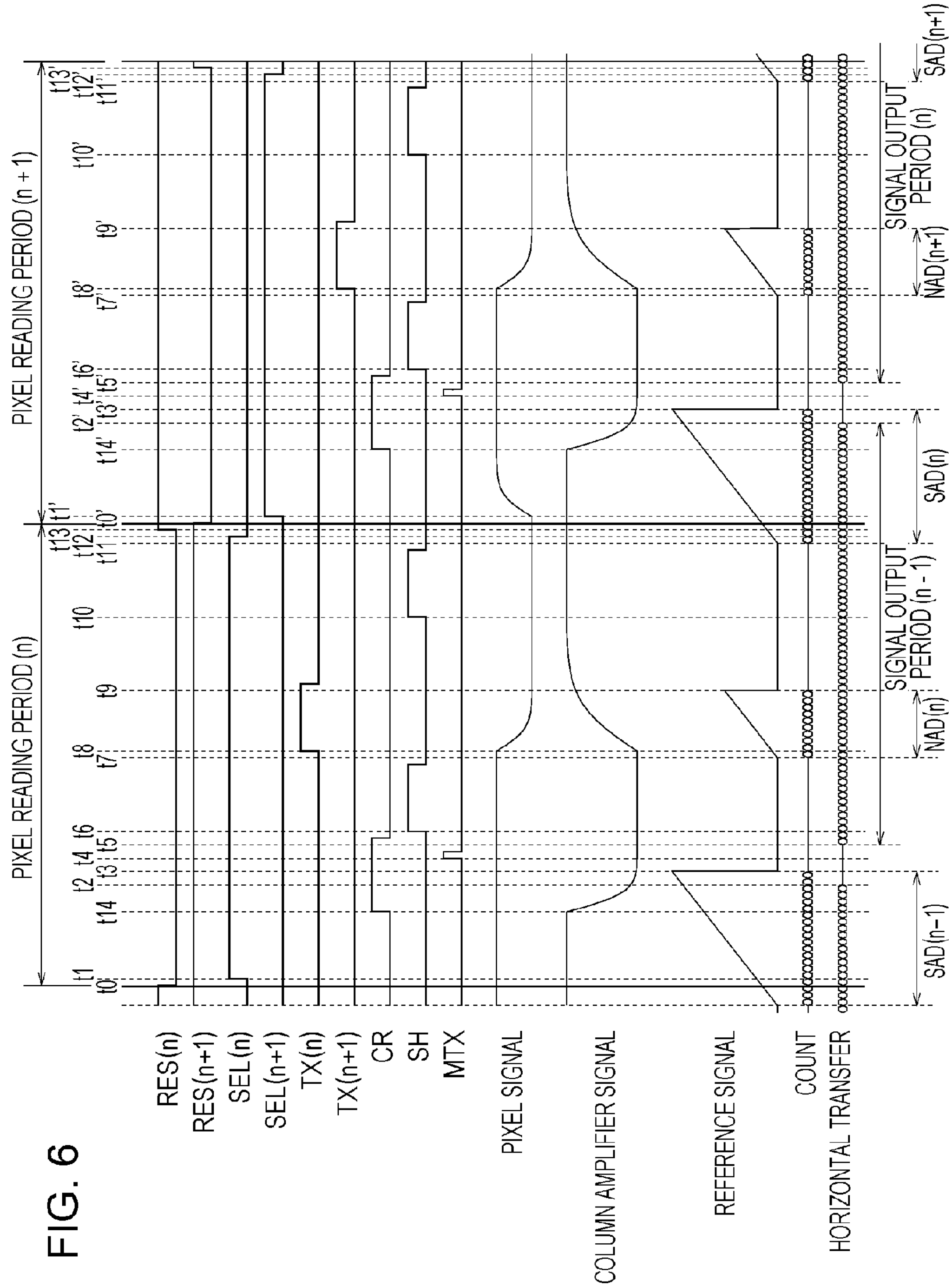

PIXEL READING PERIOD (n)
PIXEL READING PERIOD (n + 1)
t0 t1 t14 t2 t3 t4 t5 t6 t7 t8 t9 t10 t11 t12 t13
t0' t1' t14' t2' t3' t4' t5' t6' t7' t8' t9' t10' t11' t12' t13'
RES(n)
RES(n+1)
SEL(n)
SEL(n+1)
TX(n)
TX(n+1)
CR
SH
MTX
PIXEL SIGNAL
COLUMN AMPLIFIER SIGNAL
REFERENCE SIGNAL
COUNT
HORIZONTAL TRANSFER
SAD(n-1)
NAD(n)
SIGNAL OUTPUT PERIOD (n - 1)
SAD(n)
NAD(n+1)
SIGNAL OUTPUT PERIOD (n)
SAD(n+1)

FIG. 7

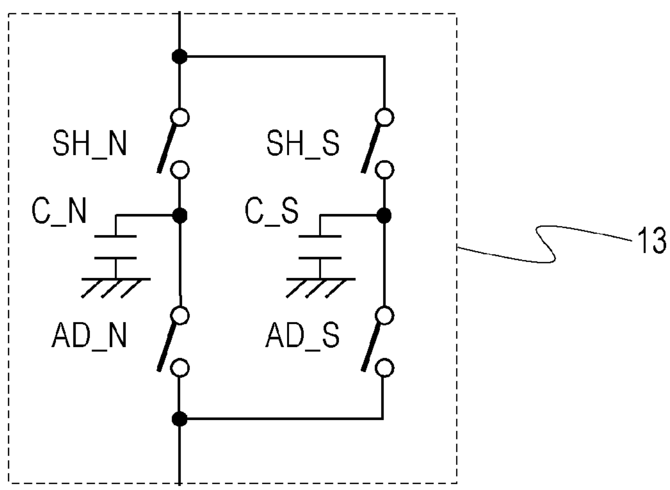
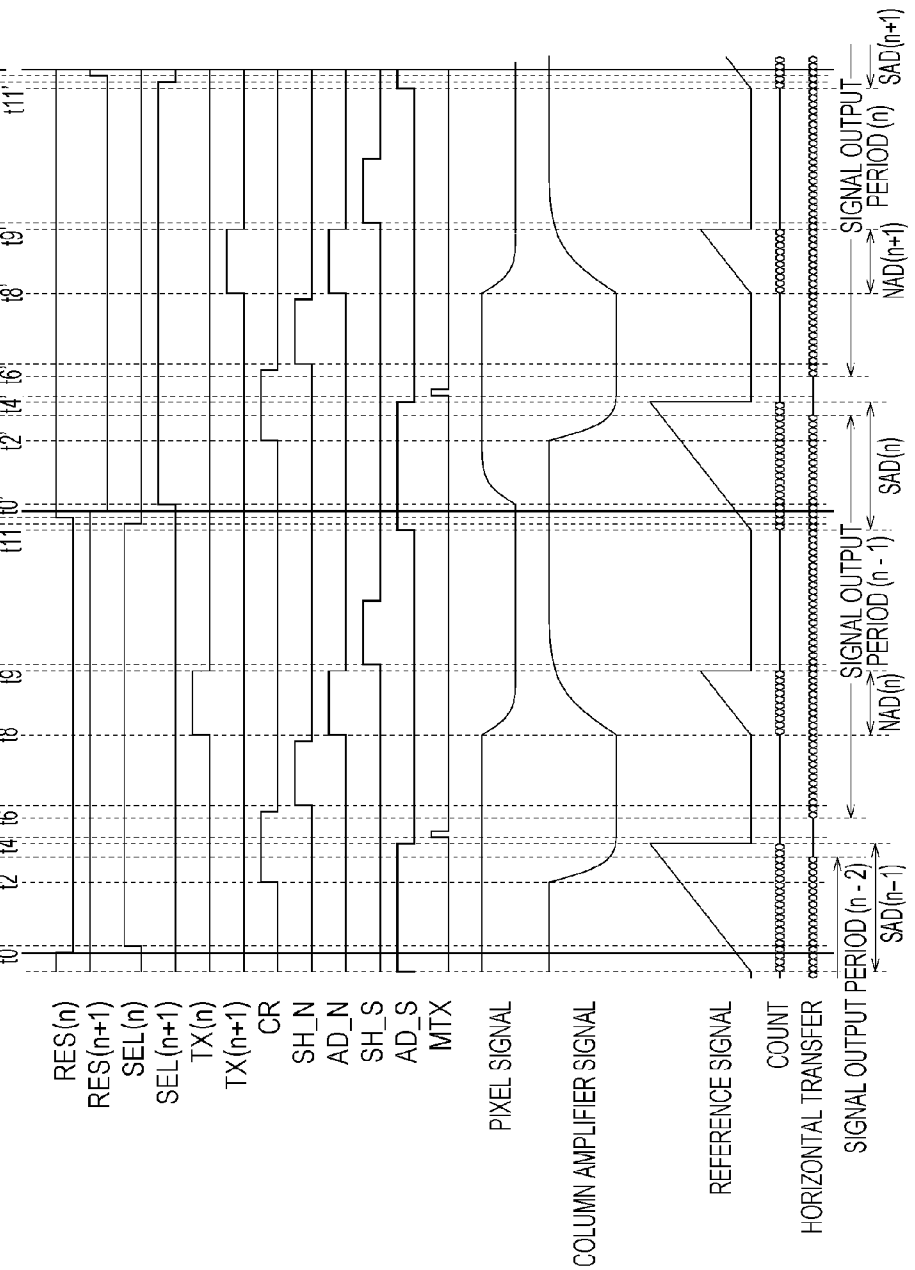


FIG. 8


PIXEL READING PERIOD (n)
PIXEL READING PERIOD (n + 1)
t0
t1
t2
t3
t4
t5
t6
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t8
t9
t10
t11
t12
t13
t0'
t1'
t2'
t3'
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t5'
t6'
t7'
t8'
t9'
t10'
t11'
t12'
t13'
RES(n)
RES(n+1)
SEL(n)
SEL(n+1)
TX(n)
TX(n+1)
CR
SH_N
AD_N
SH_S
AD_S
MTX
PIXEL SIGNAL
COLUMN AMPLIFIER SIGNAL
REFERENCE SIGNAL
COUNT
HORIZONTAL TRANSFER
SIGNAL OUTPUT PERIOD
SAD(n−1)
SIGNAL OUTPUT PERIOD (n - 2)
NAD(n)
SIGNAL OUTPUT PERIOD (n - 1)
SAD(n)
NAD(n+1)
SIGNAL OUTPUT PERIOD (n)
SAD(n+1)

FIG. 9

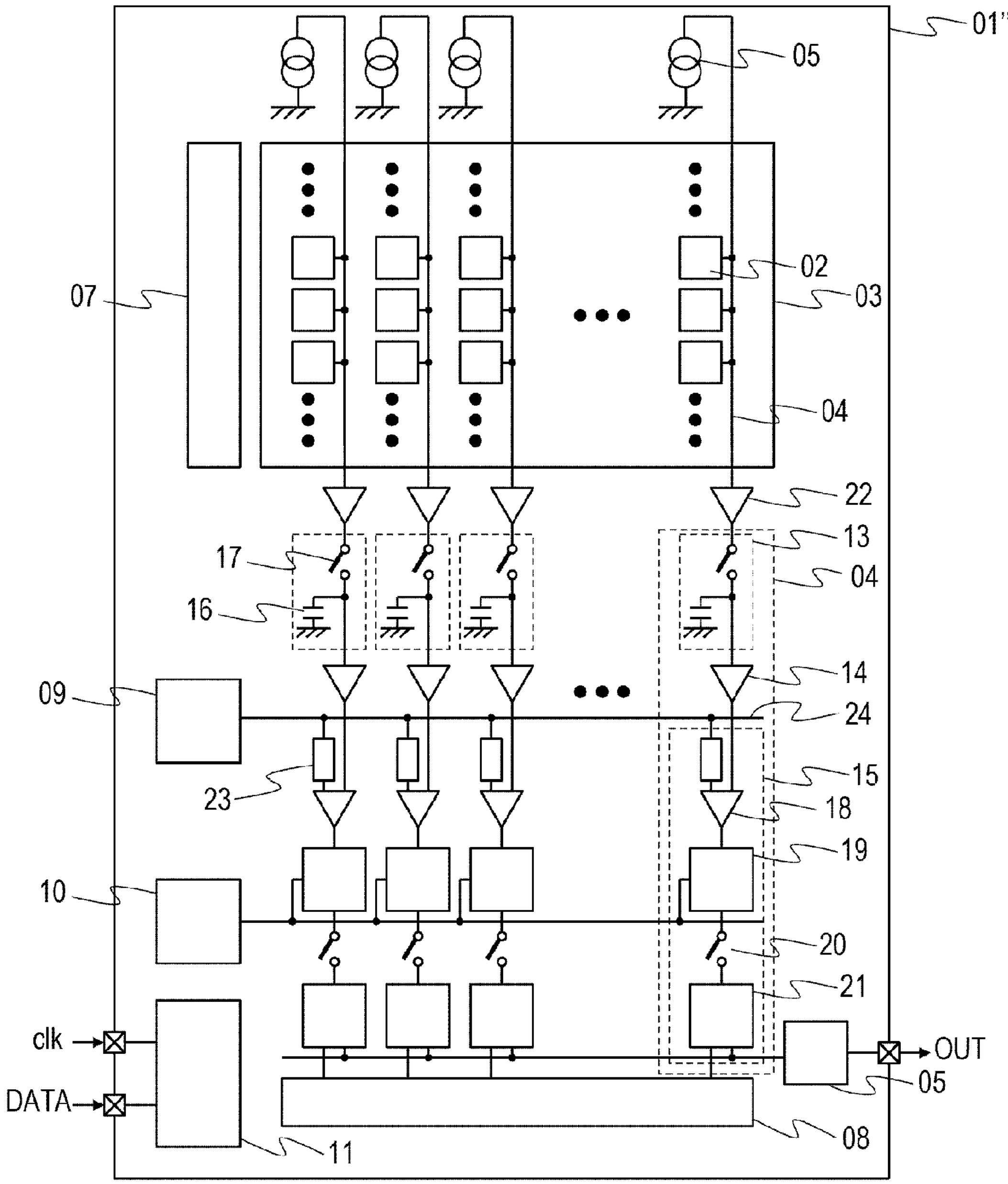
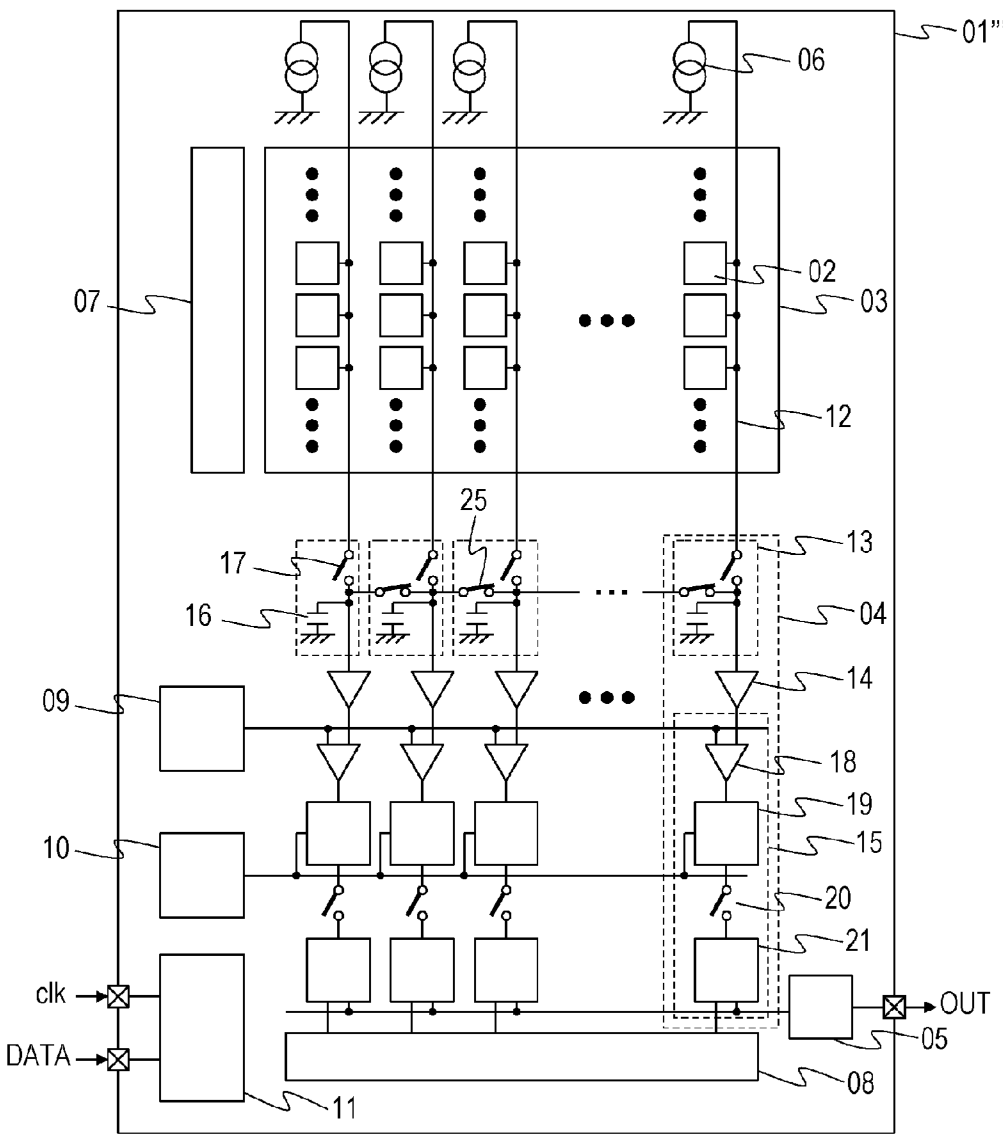

01"
05
02
03
07
04
22
13
17
04
16
14
09
24
23
15
18
19
10
20
21
clk
DATA
OUT
05
08
11

FIG. 10


01'''
06
07
02
03
12
25
13
17
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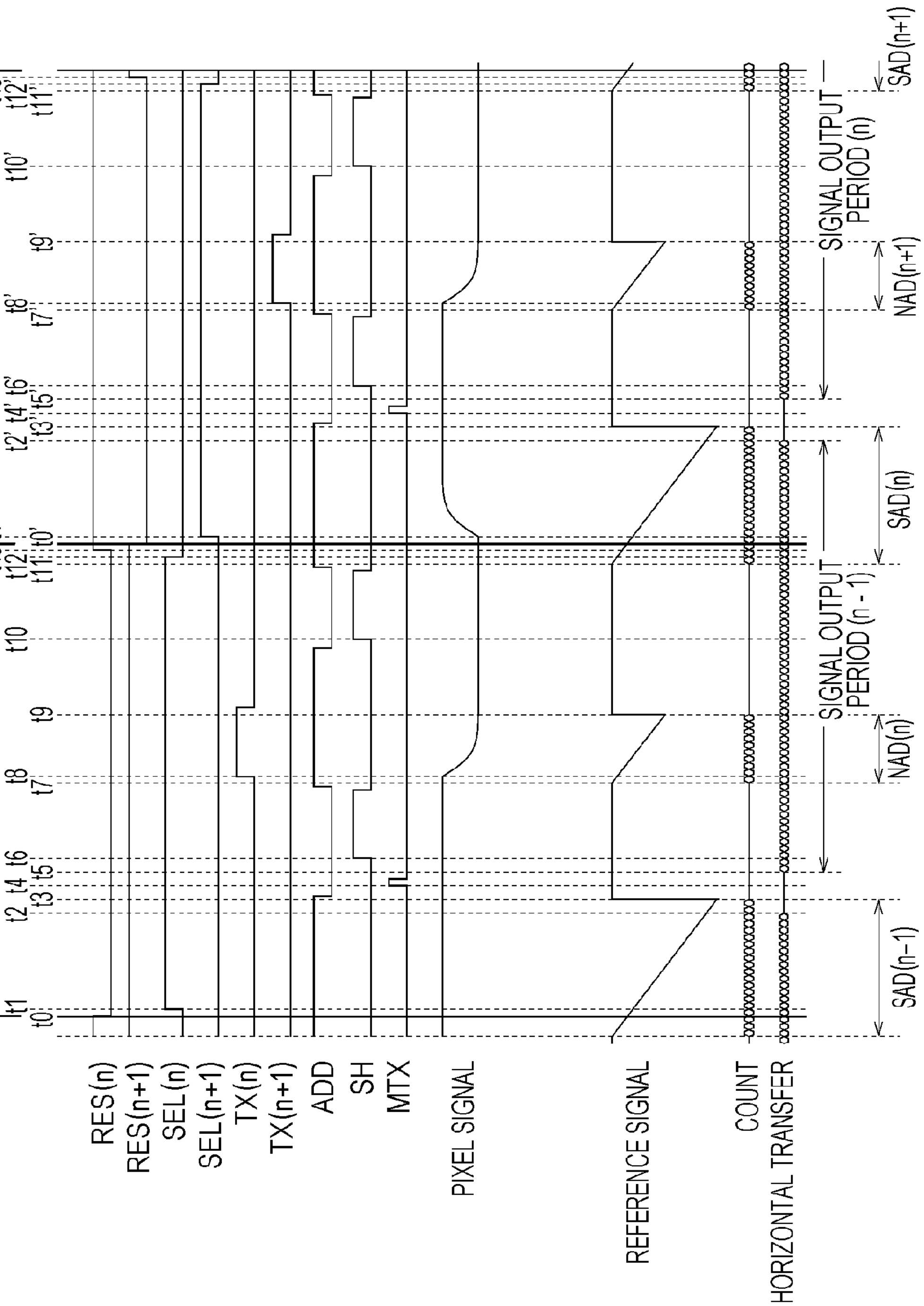
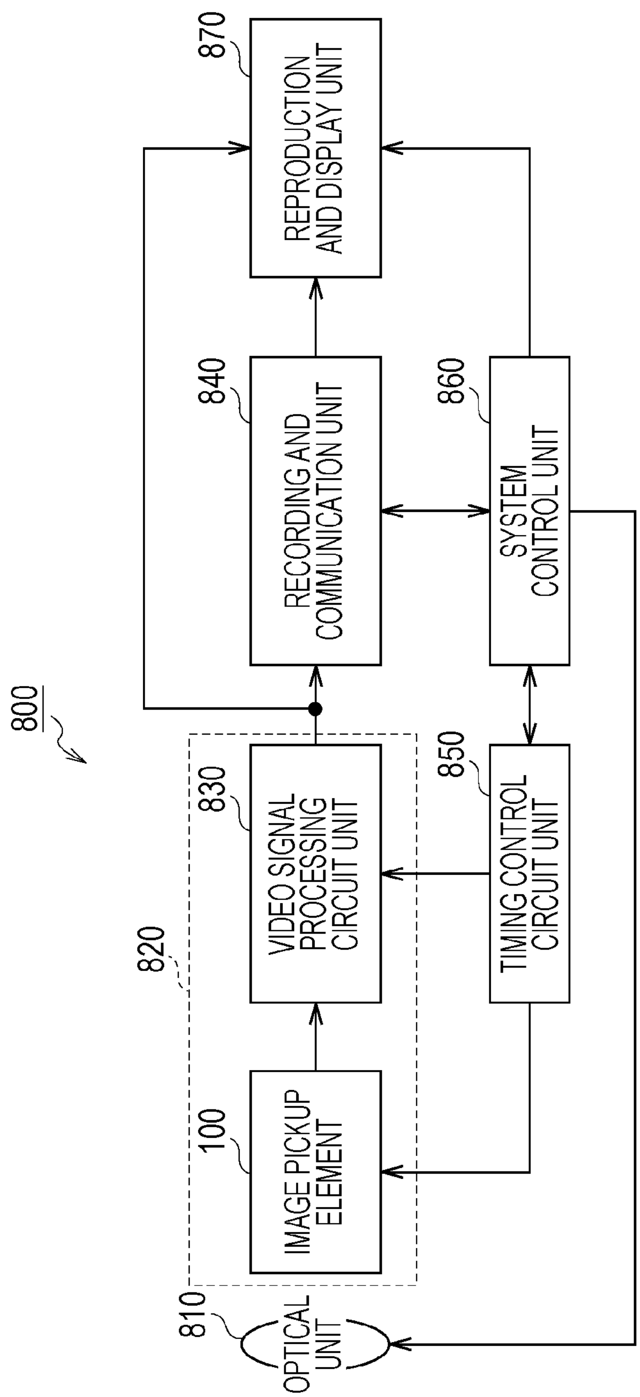
14
09
18
19
10
15
20
21
clk
DATA
OUT
05
08
11

FIG. 11



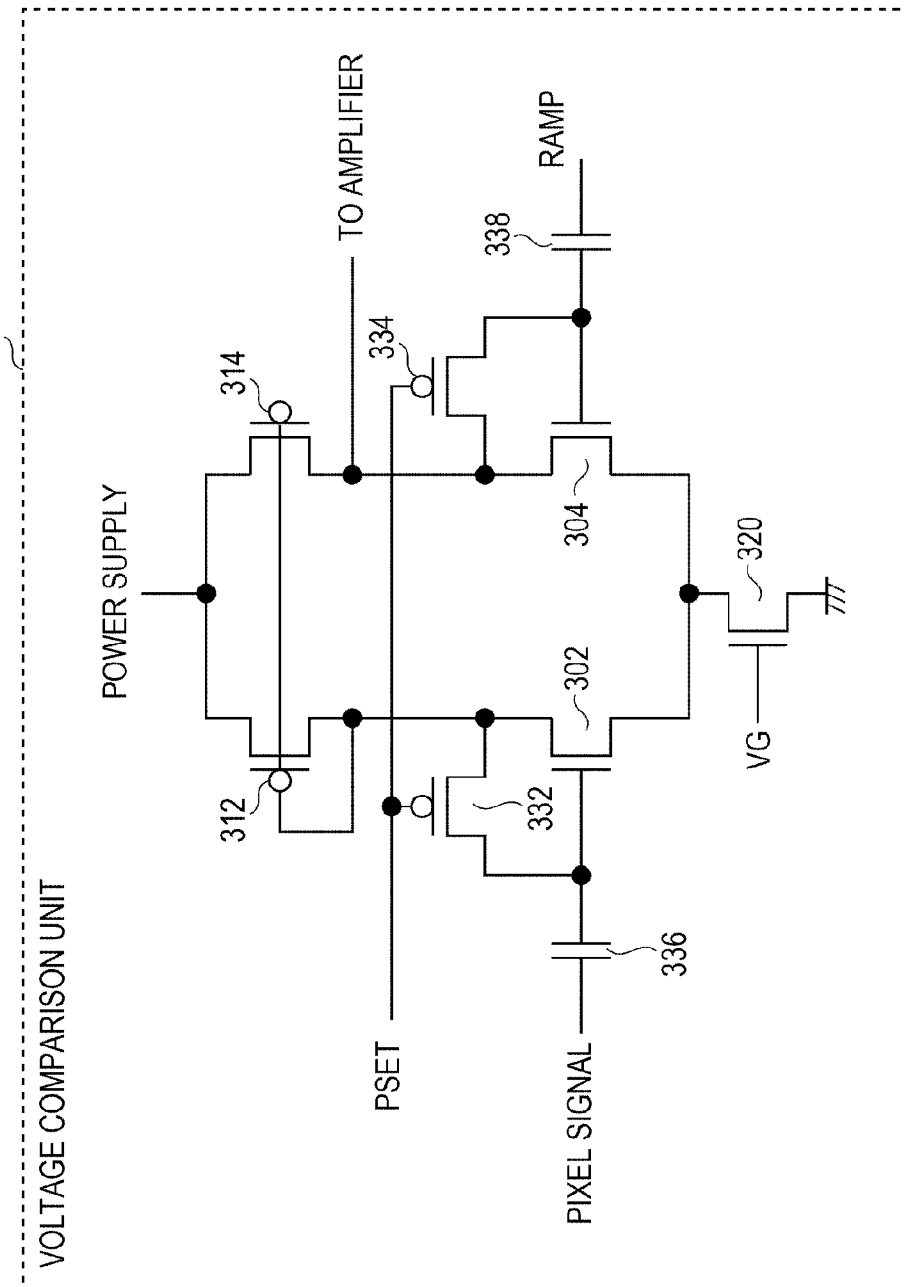
PIXEL READING PERIOD (n)
PIXEL READING PERIOD (n + 1)
RES(n)
RES(n+1)
SEL(n)
SEL(n+1)
TX(n)
TX(n+1)
ADD
SH
MTX
PIXEL SIGNAL
REFERENCE SIGNAL
COUNT
HORIZONTAL TRANSFER
t0 t1 t2 t3 t4 t5 t6 t7 t8 t9 t10 t11 t12 t13
t0' t1' t2' t3' t4' t5' t6' t7' t8' t9' t10' t11' t12' t13'
SAD(n−1)
NAD(n)
SIGNAL OUTPUT PERIOD (n - 1)
SAD(n)
NAD(n+1)
SIGNAL OUTPUT PERIOD (n)
SAD(n+1)

FIG. 12


800
870
REPRODUCTION AND DISPLAY UNIT
840
RECORDING AND COMMUNICATION UNIT
860
SYSTEM CONTROL UNIT
830
VIDEO SIGNAL PROCESSING CIRCUIT UNIT
850
TIMING CONTROL CIRCUIT UNIT
820
100
IMAGE PICKUP ELEMENT
810
OPTICAL UNIT

Prior Art

FIG. 13



PHOTOELECTRIC CONVERSION APPARATUS AND IMAGE PICKUP SYSTEM INCLUDING AN AD CONVERSION UNIT TO CONVERT A SIGNAL INTO A DIGITAL SIGNAL

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a photoelectric conversion apparatus and an image pickup system.

2. Description of the Related Art

It is known that an analog-to-digital (AD) converter is provided for each column of a pixel array in a solid-state image pickup apparatus. Japanese Patent Laid-Open No. 2009-10787 describes a configuration in which a signal holding switch and a signal holding capacitance directly connected to the AD converter are provided upstream of the AD converter provided in each column of the pixel array. According to Japanese Patent Laid-Open No. 2009-10787, a read operation for an analog signal from a pixel, and an AD conversion operation thereof are performed in parallel by turning off the signal holding switch during an AD conversion period for the analog signal held in the signal holding switch, so that high-speed reading can be realized.

However, the configuration described in Japanese Patent Laid-Open No. 2009-10787 could cause a fixed pattern noise for each column. A reason for this noise generation will be described below.

FIG. **13** is a diagram taken from FIG. 8 of Japanese Patent Laid-Open No. 2009-10787 and illustrates a circuit configuration of a voltage comparison unit **252** included in the AD conversion unit. In this circuit, when a relationship of magnitude between a “pixel signal” and a “RAMP” corresponding to input signals to the voltage comparison unit **252** is reversed (in other words when the “pixel signal” being smaller than “RAMP” changes to become greater than “RAMP” as “RAMP” decreases with time), a voltage at a drain of a transistor **314** corresponding to an output of the voltage comparison unit **252** is changed from a high level to a low level or from the low level to the high level. This change also affects a gate of the transistor **314** via a gate-drain capacitance of the transistor **314**. Further, since a gate and a drain of the transistor **312** are connected to the gate of the transistor **314**, the change caused in the drain of the transistor **314** also affects the gate and the drain of the transistor **312**. Furthermore, since the drain of the transistor **312** is connected to a drain of a transistor **302** that is an input transistor of the voltage comparison unit **252**, the change caused in the drain of the transistor **312** also affects a gate of the transistor **302**. Accordingly, a phenomenon in which an output of the voltage comparison unit **252** affects the “pixel signal” corresponding to an input of voltage occurs.

According to the configuration described in Japanese Patent Laid-Open No. 2009-10787, the “pixel signal” is directly connected to the signal holding capacitance and is electrically disconnected from a unit pixel during the AD conversion period. Accordingly, a transient change of a drain voltage of the transistor **314** which is caused during the AD conversion period also changes a signal voltage of the signal held in the signal holding capacitance. That is, since the signal voltage of the signal held in the signal holding capacitance may be a voltage different from the voltage originally held, a value of digital data obtained as a result of the AD conversion may be an inaccurate value. In addition, an influence imposed on the “pixel signal” by the change of the drain voltage of the transistor **314** varies for each column because of variations in manufacturing the voltage comparison units **252**, and this becomes fixed pattern noise for each column.

SUMMARY OF THE INVENTION

A photoelectric conversion apparatus according to an aspect of the present invention includes a pixel array in which a plurality of pixels are arranged in a matrix and column signal processing units provided in correspondence with respective columns of the pixel array, in which the column signal processing unit includes a sample-and-hold unit configured to hold a signal output from the pixel, a buffer unit configured to buffer the signal held in the sample-and-hold unit, and an AD conversion unit, and the AD conversion unit converts the signal held by the sample-and-hold unit and buffered by the buffer unit into a digital signal.

Further features of the present invention will become apparent from the following description of embodiments with reference to the attached drawings. Each of the embodiments of the present invention described below can be implemented solely or as a combination of a plurality of the embodiments or features thereof where necessary or where the combination of elements or features from individual embodiments in a single embodiment is beneficial.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a block diagram illustrating a configuration of a photoelectric conversion apparatus.

FIG. **2** is an equivalent circuit diagram illustrating a configuration of a pixel.

FIG. **3** is a timing chart for describing an operation by the photoelectric conversion apparatus.

FIG. **4** is a block diagram illustrating a configuration of another photoelectric conversion apparatus.

FIG. **5** is an equivalent circuit diagram illustrating a configuration of an inverting amplifier.

FIG. **6** is a timing chart for describing an operation by the photoelectric conversion apparatus.

FIG. **7** is an equivalent circuit diagram illustrating a configuration of a sample-and-hold unit.

FIG. **8** is a timing chart for describing an operation by the photoelectric conversion apparatus.

FIG. **9** is a block diagram illustrating a configuration of another photoelectric conversion apparatus.

FIG. **10** is a block diagram illustrating a configuration of another photoelectric conversion apparatus.

FIG. **11** is a timing chart for describing an operation by the photoelectric conversion apparatus.

FIG. **12** is a block diagram illustrating a configuration of an image pickup system.

FIG. **13** illustrates FIG. 8 of Japanese Patent Laid-Open No. 2009-10787.

DESCRIPTION OF THE EMBODIMENTS

Embodiments

With reference to the drawings, embodiments of the present invention will be described.

First Embodiment

A photoelectric conversion apparatus **01** according to a first embodiment includes a pixel array **03** in which a plurality of pixels **02** are arranged in a matrix, column signal processing units **04**, a data output unit **05**, and load current sources **06**.

The photoelectric conversion apparatus **01** further includes a vertical scanning unit **07** that controls operations of the pixels **02** in units of rows, a horizontal scanning unit **08**, a reference signal generation unit **09**, a count unit **10**, and a control unit **11**. The pixels **02** in each column are connected to the column signal processing unit **04** and the load current source **06** via a pixel output line **12**. Each of the column signal processing units **04** includes a sample-and-hold unit **13**, a buffer unit **14**, and an analog-to-digital (AD) conversion unit **15**.

The control unit **11** receives a clock signal "clk" and communication data "data" from outside of the apparatus and controls operations of the respective blocks included in the photoelectric conversion apparatus **01**.

The sample-and-hold unit **13** includes a capacitor element **16** and a switch **17**, and when the switch **17** is switched from on to off, a signal appearing on the pixel output line **12** is held in the capacitor element **16**. The capacitor element **16** is connected to the AD conversion unit **15** via the buffer unit **14**.

The AD conversion unit **15** includes a comparison unit **18**, a write memory **19**, an inter-memory transfer switch **20**, and a read memory **21**. The comparison unit **18** receives a reference signal supplied from the reference signal generation unit **09** and an output of the buffer unit **14** as input signals, and when a relationship of magnitude between those input signals is reversed, a logic level of an output of the comparison unit **18** is reversed. When the logic level of the output of the comparison unit **18** is reversed, the write memory **19** holds a count signal supplied from the count unit **10**. The count signal held in the write memory **19** is transferred to the read memory **21** via the inter-memory transfer switch **20**. When the signal held in the read memory **21** is selected by the horizontal scanning unit **08**, the signal is transmitted to the data output unit **05**. According to the present embodiment, each of the write memory **19** and the read memory **21** has a configuration in which two pieces of digital data can be held independently.

FIG. **2** is an equivalent circuit diagram for describing a configuration example of the pixel **02**. The pixel **02** includes a photodiode PD as a photoelectric conversion unit, a transfer transistor TX, a source follower transistor SF, a reset transistor RES, and a selection transistor SEL.

Charges generated through a photoelectric conversion by the photodiode PD are transferred to a gate node of the source follower transistor SF via the transfer transistor TX. When the selection transistor SEL is turned on, the source follower transistor SF functions as a source follower circuit together with the load current source **06**, and an output in accordance with the charge amount transferred to the gate node appears on the pixel output line **12**. When the reset transistor RES is turned on, the reset transistor RES resets the gate node of the source follower transistor SF to a power supply voltage.

Next, by further referring to FIG. **3**, an operation of the photoelectric conversion apparatus **01** according to the present embodiment will be described. The following description focuses on operations relating to the pixels in an n-th row (n is an integer higher than or equal to 1) and an (n+1)-th row in the pixel array **03**. In FIG. **3**, signals RES(n), SEL(n), and TX(n) respectively indicate signals supplied to gates of the reset transistor RES, the selection transistor SEL, and the transfer transistor TX of the pixel in the n-th row. The same applies to signals RES(n+1), SEL(n+1), and TX(n+1). These signals are supplied from the vertical scanning unit **07**. A signal SH is a signal for controlling a conducting state of the sample-and-hold switch **17**, and a signal MTX is a signal for controlling a conducting state of the inter-memory transfer switch **20**. The following description will be given based on the assumption that when the respective signals are at the high level, the corresponding transistors or switches are turned on.

According to the present embodiment, an operation example in which at least two of a sample-and-hold operation of the analog signal output from the pixel **02**, an AD conversion operation, and a signal output operation from the read memory **21** are performed in parallel will be described.

A period from a time t0 to a time t0' corresponds to a period in which the analog signal related to the pixel in the n-th row is held in the capacitor element **16** (PIXEL READING PERIOD (n) in FIG. **3**).

At the time t0, since the signal RES(n) is switched from the high level to the low level, the reset transistor RES of the pixel in the n-th row is turned off. Accordingly, a reset state of the source follower transistor SF is cancelled.

When the signal SEL(n) turns to the high level at a time t1, the selection transistor SEL of the pixel in the n-th row is turned on, and a signal corresponding to the reset of the gate node of the source follower transistor SF of the pixel in the n-th row appears on the pixel output line **12**. This output contains noise generated when the reset transistor RES is turned off and noise derived from the source follower transistor SF. Hereinafter, this output will be referred to as N signal.

During a period up to a time t2, a horizontal transfer operation, in which a digital signal related to the N signal of the pixel in the (n−1)-th row is transferred from the read memory **21** to the data output unit **05**, is performed. In FIG. **3**, the horizontal transfer operation is started at a time before the time t0, but depending on conditions such as the number of the read memories **21** or an operating frequency of the horizontal scanning unit **08**, the horizontal transfer operation may be started at the time t0 or later.

A period up to a time t3 is a period in which a signal component of the pixel in the (n−1)-th row which is held in the capacitor element **16** is converted into a digital signal (a period SAD(n−1) in FIG. **3**). During this period, the capacitor element **16** is electrically cut off from the pixel output line **12** by the switch **17**. In response to the temporally-varying relationship of magnitude between the reference signal and the output of the buffer unit **14**, when the relationship of magnitude between those is reversed, the comparison unit **18** causes the write memory **19** to hold a count value of the count unit **10** at that time. In FIG. **3**, the period SAD(n−1) is started at a time before the time t0, but depending on conditions such as a resolution of the AD conversion unit **15** or the operating frequency, the period SAD(n−1) may be started at the time t0 or later.

At a time t4, the signal MTX turns to the high level, and two digital signals held in the write memory **19** during a period NAD(n−1) and the period SAD(n−1) are transferred to the read memory **21**.

From a time t5 to a time t2', the horizontal transfer operation in which the digital signal obtained by the AD conversion during the period SAD(n−1) is output from the read memory **21** is performed.

From a time t6, since the signal SH temporarily turns to the high level, the N signal related to the pixel in the n-th row which is output to the pixel output line **12** is held in the capacitor element **16**.

During a period from a time t7 to a time t9, an operation of converting the N signal in the n-th row into a digital signal is performed (a period NAD(n) in FIG. **3**). During the period NAD(n), since the signal SH is at the low level, the capacitor element **16** is in a state of being electrically cut off from the pixel output line **12**.

From a time t8, since the signal TX(n) temporarily turns to the high level, the charges accumulated by this time in the photodiode PD of the pixel in the n-th row are transferred to the gate node of the source follower transistor SF. A potential at the pixel output line **12** fluctuates in accordance with the transferred charge amount. A signal equivalent to a sum of a signal in accordance with the charge amount generated by the photoelectric conversion in the photodiode PD and the N signal output from the pixel **02** at the time t1 is output to the pixel output line **12** at this time. Hereinafter, this signal is referred to as (S+N) signal.

From a time t10, since the signal SH temporarily turns to the high level, the (S+N) signal related to the pixel in the n-th row which is output to the pixel output line **12** is held in the capacitor element **16**.

From a time t11 to a time t3', an operation of converting the (S+N) signal related to the pixel in the n-th row into a digital signal is performed (a period SAD(n) in FIG. **3**). During the period SAD(n), since the signal SH is at the low level, the capacitor element **16** is in a state of being electrically cut off from the pixel output line **12**.

At a time t12, the signal SEL(n) turns to the low level, and the selection transistor SEL of the pixel in the n-th row is turned off.

At a time t13, the signal RES(n) turns to the high level, and causes the gate node of the source follower transistor SF of the pixel in the n-th row to be in a reset state.

An operation during a pixel reading period (n+1) that starts from the time t0' is similar to the operation during the pixel reading period (n), and therefore a description thereof will be omitted.

The digital signals obtained during the period NAD(n) and the period SAD(n) are subjected to differential processing by the data output unit **05** or a signal processing unit that is not illustrated and provided downstream of the data output unit **05**. Accordingly, correlated double sampling (CDS) processing for reducing the N signal is performed.

As described above, during the AD conversion period, the capacitor element **16** is electrically cut off from the pixel array **03**, and in a state in which the signal is held, the signal held in the capacitor element **16** is supplied to the AD conversion unit **15** via the buffer unit **14**. Since the buffer unit **14** is in a state of driving an input node of the comparison unit **18**, it is possible to suppress a phenomenon where a transient change of the output of the comparison unit **18** fluctuates the input of the comparison unit **18**, and it is possible to reduce the fixed pattern noise that may have been generated in the conventional configuration. Particularly, a capacitor element in which a reference voltage (GND in the present embodiment) is supplied to one of nodes is used, and it is therefore possible to further suppress the fixed pattern noise as compared to a case where the capacitor element connected in series to the signal path is used for the sample-and-hold unit **13**.

In addition, as described above, according to the present embodiment, since the AD conversion operation and the horizontal transfer operation are performed in parallel during a period in which the analog signal is read out from the pixel in a certain row, it is possible to realize reading at a high speed.

According to the present embodiment, the fixed pattern noise is reduced, and further it is possible to realize high-speed reading.

Second Embodiment

FIG. **4** is a block diagram illustrating a configuration of a photoelectric conversion apparatus **01'** according to the present embodiment. The difference from FIG. **1** resides in that a column amplifier **22** is provided between the pixels **02** and the column signal processing unit **04**.

An amplifier that can set an amplification factor exceeding 1×, for example, can be used for the column amplifier **22**. FIG. **5** is an equivalent circuit diagram of an inverting amplifier circuit using a differential amplifier as an example of the configuration of the column amplifier **22**. An operation amplifier, for example, can be used for the differential amplifier.

The inverting amplifier circuit in FIG. **5** includes a differential amplifier OP, an input capacitance Cin, a feedback capacitance Cf, and a feedback switch CR. The differential amplifier OP receives a reference voltage VCR at a non-inversion input terminal thereof, and one node of the input capacitance Cin, one node of the feedback capacitance Cf, and one node of the feedback switch CR are connected to an inversion input terminal. The other node of the input capacitance Cin is connected to the pixel **02** and the load current source **06** via the pixel output line **12**. The other node of the feedback capacitance Cf and the other node of the feedback switch CR are both connected to an output terminal of the differential amplifier OP. An output of the column amplifier **22** is connected to the switch **17**. According to this configuration, the amplitude factor of the column amplifier **22** is determined by a ratio of a capacitance value of the input capacitance Cin to a capacitance value of the feedback capacitance Cf. Furthermore, according to the illustrated configuration, CDS processing for reducing the noise generated in the pixel **02** can also be performed.

FIG. **6** is a timing chart for describing an operation according to the present embodiment. The difference from the operation described in FIG. **3** resides in that a signal CR for controlling the feedback switch CR is added, and a direction of a change in the level of the reference signal is reversed in correspondence with the use of an inverting amplifier for the column amplifier **22**. The operation according to the present embodiment will be described by mainly focusing on the difference from the operation described in FIG. **3**.

In FIG. **6**, from a time t14 that is between the time t1 and the time t3, the signal CR temporarily turns to the high level. Accordingly, the column amplifier **22** operates as a voltage follower, and also the N signal of the pixel in the n-th row appearing on the pixel output line **12** at this time is held in the input capacitance. The signal held in the capacitor element by the operation from the time t6 is not the N signal of the pixel but is a signal equivalent to an offset of the column amplifier **22**. Therefore, during the period NAD(n), an offset component of the column amplifier **22** is converted into a digital signal.

After the signal CR turns to the low level, when the (S+N) signal of the pixel in the n-th row appears on the pixel output line **12**, the column amplifier **22** outputs a signal in which a fluctuation amount based on the N signal being set as a reference, that is, a component equivalent to the S signal is amplified. As a result, the signal held in the capacitor element **16** by the operation from the time t10 turns to a signal obtained by superposing the signal to which the S signal of the pixel in the n-th row is amplified, on the offset component of the column amplifier. This signal is converted into a digital signal during the period SAD(n).

Similarly to the first embodiment, according to the present embodiment, a difference between the digital signal obtained during the period NAD(n) and the digital signal obtained during the period SAD(n) is obtained by the data output unit **05**, or the signal processing unit provided downstream of the data output unit **05**. Accordingly, the digital signal in which the offset component of the column amplifier is reduced can be obtained.

According to the present embodiment, the column amplifier **22** is provided upstream of the sample-and-hold unit **13**, and the signal is amplified by the column amplifier **22**. Accordingly, it is possible to improve a signal-to-noise (S/N) ratio of the obtained signal. As the amplitude factor of the column amplifier **22** is higher, it is possible to further reduce an influence of the noise component derived from charge injection that is caused when sampling and holding of the signal are performed by the sample-and-hold unit **13**.

In a case where the column amplifier **22** is constituted as an amplifier in which the amplitude factor is variable, the amplitude factor of the column amplifier **22** may be changed on the basis of image pickup conditions or a sensitivity that is set depending on an image pickup system.

According to the present embodiment described above, the fixed pattern noise is reduced, and further it is possible to realize high-speed reading. Furthermore, the S/N ratio of the signal can be improved as compared to the first embodiment.

Third Embodiment

In the respective embodiments described above, the configuration in which the sample-and-hold unit **13** is provided with one pair of the capacitor element **16** and the switch **17** has been described. However, the sample-and-hold unit **13** may adopt other configurations.

FIG. **7** illustrates a configuration of the sample-and-hold unit **13** according to the present embodiment. The sample-and-hold unit **13** according to the present embodiment includes a two-system sample-and-hold circuit. A capacitor element C_N is a capacitor element configured to hold the N signal or the offset component of the column amplifier **22** as described above in the respective embodiments. On the other hand, a capacitor element C_S is a capacitor element configured to hold the (S+N) signal and the signal obtained by superposing the amplified S signal on the offset component of the column amplifier **22** described in the above respective embodiments. According to this configuration, during the period in which the AD conversion of the signal held in one of the two capacitor elements provided to the sample-and-hold unit **13** is performed, it is possible to cause the other capacitor element to hold the output of the column amplifier **22**. Also in a case where the sample-and-hold unit is provided with three or more capacitor elements, the operation of converting the signal held in one capacitor element into a digital signal and the operation of causing another one of capacitor elements to hold the signal output from the pixel can be performed in parallel.

FIG. **8** is a timing chart for describing an operation according to the present embodiment. Herein, a case in which the sample-and-hold unit **13** of the photoelectric conversion apparatus **01'** described in the second embodiment is replaced by the configuration illustrated in FIG. **7** will be described as an example. Signals SH_N, AD_N, SH_S, and AD_S in FIG. **8** are signals for controlling the respective switches having the same reference symbols illustrated in FIG. **7**, and the corresponding switch is turned on when the signal is at the high level.

From the time t0, the pixel reading period in the n-th row starts. According to the present embodiment, the time t0 is a timing within the signal output period (n−2) related to the pixel in the (n−2)-th row and within the AD conversion period SAD(n−1) related to the pixel in the (n−1)-th row. During the period SAD(n−1), the signal AD_S is at the high level so that the AD conversion of the signal held in the capacitor element C_S is performed. First, since the signal RES(n) is switched from the high level to the low level, the reset transistor RES of the pixel in the n-th row is turned off. Accordingly, the reset state of the source follower transistor SF is cancelled.

When the signal SEL(n) turns to the high level at the time t1, the selection transistor SEL of the pixel in the n-th row is turned on, and a signal corresponding to the reset of the gate node of the source follower transistor SF of the pixel in the n-th row appears on the pixel output line **12**. This output contains the noise generated when the reset transistor RES is turned off and the noise derived from the source follower transistor SF. Hereinafter, this output will be referred to as N signal.

At the time t2, when the signal CR turns to the high level, the feedback switch CR of the column amplifier **22** is turned on, so that both the nodes of the feedback capacitance Cf are reset. Thereafter, when the signal CR turns to the low level, the level appearing on the pixel output line **12** at that time can be clamped in the input capacitance Cin. According to the present embodiment, the above described N signal is clamped.

At the time t3, the signal output period related to the pixel in the (n−2)-th row ends.

At the time t4, the AD conversion period SAD(n−1) related to the pixel in the (n−1)-th row ends. Along with this, the signal AD_S turns to the low level, and a switch AD_S is turned off.

At the time t5, when the signal MTX turns to the high level, the digital signals held in the write memory **19** up to this time are transferred to the read memory **21** via the inter-memory transfer switch **20**. More specifically, the digital signal obtained during the period NAD(n−1) that is not illustrated and the digital signal obtained during the period SAD(n−1) are transferred.

From the time t6, the horizontal scanning unit **08** starts scanning of the read memory **21**, and the signal output period with regard to the pixel in the (n−1)-th row starts.

From the time t7, when the signal SH_N temporarily turns to the high level, the output of the column amplifier **22** is held in the capacitor element C_N. The output held at this time is a signal corresponding to the reset of the column amplifier **22**, and the signal has the offset of the column amplifier **22** as a main component.

From the time t8, since the signal TX(n) temporarily turns to the high level, the charges accumulated in the photodiode PD are transferred to the gate node of the source follower transistor SF.

At the same time t8, the signal AD_N also turns to the high level, so that the signal held in the capacitor element C_N is supplied to the AD conversion unit **15** via the buffer unit **14**. A period from the time t8 to the time t9 is the AD conversion period NAD(n) related to the pixel in the n-th row. The digital signal obtained during this period corresponds to the signal having the offset of the column amplifier **22** as the main component which is obtained by the operation from the time t7.

From the time t10, the signal SH_S temporarily turns to the high level, so that the signal output from the column amplifier **22** at this time is held in the capacitor element C_S. Specifically, the signal is a signal obtained by superposing the signal which corresponds to the charge amount transferred to the gate node of the source follower transistor SF by the operation from the time t8 and which is amplified by the column amplifier **22**, on the signal obtained by the operation from the time t7.

At the time t11, when the signal AD_S turns to the high level, the AD conversion period SAD(n) related to the pixel in the n-th row starts.

At the time t12, the signal SEL(n) turns to the low level, and the selection transistor SEL of the pixel in the n-th row is turned off.

At a time t18, the signal RES(n) turns to the high level, and the gate node of the source follower transistor SF of the pixel in the n-th row is in a reset state.

The operation during the pixel reading period (n+1) that starts from the time t0' is similar to the operation during the pixel reading period (n), and therefore a description thereof will be omitted.

The digital signals obtained during the period NAD(n) and the period SAD(n) are subjected to differential processing by the data output unit **05**, or the signal processing unit which is not illustrated and which is provided downstream of the data output unit **05**. Accordingly, the correlated double sampling (CDS) processing for reducing the N signal is performed.

According to the present embodiment, during the period in which the AD conversion of the signal held in one of the two capacitor elements provided to the sample-and-hold unit **13** is performed, it is possible to cause the other capacitor element to hold the output of the column amplifier **22**. Accordingly, the operation can be performed at a still higher speed as compared to the first and second embodiments.

In the present embodiment, the case in which the signal TX(n) or TX(n+1) is transited at the same time as the signal AD_N has been described, but the timing is not limited to this timing.

Fourth Embodiment

FIG. **9** is a block diagram illustrating a configuration of a photoelectric conversion apparatus **01"** according to the present embodiment. The difference from FIG. **4** resides in that reference signal buffer units **23** are added. Hereinafter, a description will be given while mainly focusing on the difference from FIG. **4**.

According to the present embodiment, the reference signal supplied from the reference signal generation unit **09** is supplied to the comparison unit **18** via the reference signal buffer unit **23** provided in each column. The reference signal buffer unit **23** functions similarly to the buffer unit **14** and suppresses influences of the fluctuation of the output of the comparison unit **18** on a reference signal supply line **24**. Since the reference signal supply line **24** is provided in common for the comparison units **18** in respective columns, it is possible to suppress the influence of the fluctuation of the output of the comparison unit **18** on other columns by providing the reference signal buffer units **23**.

With the configuration according to the present embodiment, buffers are provided to both the inputs of the comparison unit **18**, and therefore it is possible to suppress the influence of the fluctuation of the output of the comparison unit **18** on both the inputs, so that the comparison unit **18** can perform still more accurate comparison operation. When the buffer unit **14** and the reference signal buffer unit **23** are set to have the same circuit format, a gain with respect to the signal held in the sample-and-hold unit **13** can be matched with a gain with respect to the reference signal.

According to the present embodiment described above, the fixed pattern noise is reduced, and further it is possible to realize high-speed reading. Furthermore, the S/N ratio of the signal can be improved as compared to the first embodiment.

Fifth Embodiment

FIG. **10** is a block diagram illustrating a configuration of a photoelectric conversion apparatus **01'''** according to the present embodiment.

The difference from FIG. **1** resides in that switches **25** are further provided as connecting portions for mutually connecting the capacitor elements **16** provided to the column signal processing units **04** in different columns. According to the present embodiment, a configuration is adopted in which adjacent capacitor elements **16** in three columns are connected to each other. By turning the switch **25** on, signals based on a plurality of pixels can be averaged. The number of mutually connected capacitor elements is not limited to three, and the number is arbitrary selected as long as capacitor elements provided to the signal processing units in some columns among the signal processing units in a plurality of columns can be short-circuited mutually. In addition, capacitor elements to be connected are not limited to the capacitor elements in adjacent columns, and the switches **25** may be provided so that the capacitor elements **16** in every other column are connected to each other. For example, in the case of a photoelectric conversion apparatus provided with a Bayer color filter, signals based on pixels provided with color filters having a same color can be averaged.

FIG. **11** is a timing chart for describing an operation according to the present embodiment. The difference from FIG. **3** resides in that a signal ADD for controlling switching of a conducting state of the switch **25** is added. Hereinafter, the description will be given while focusing on the difference from the operation according to the timing chart illustrated in FIG. **3**.

By the time t6, the signal ADD turns to the low level, and the capacitor elements **16** that have been mutually short-circuited up to that time are separated from each other.

During a period between the time t7 and the time t8, when the signal ADD turns to the high level, the switch **25** is turned on, and the capacitor elements **16** in the adjacent three columns are connected to a common node. Accordingly, the N signals based on the three pixels are averaged. The AD conversion of the averaged N signal is performed during the period NAD(n).

Thereafter, during a period between the time t9 and the time t10, the switch **25** is turned off by turning the signal ADD to the low level.

Thereafter, after the signal SH that has turned to the high level from the time t10 turns to the low level, the signal ADD again turns to the high level during a period until the time t11. Accordingly, S signals based on the three pixels are averaged. The AD conversion of the averaged S signal is performed during the period SAD(n).

Thereafter, from the time t4 to the time t7 during the pixel reading period (n+1), the signal ADD turns to the low level.

By the operation according to the present embodiment, the amount of data output during the signal output period can be decreased as compared to the first embodiment. According to the present embodiment, since signals in three columns are averaged, data from only one of the three adjacent columns may be output to the data output unit **05**. Furthermore, with regard to the column signal processing units **04** in the columns from which data is not output, the buffer unit **14** and the AD conversion unit **15** may be switched to a power saving state.

According to the present embodiment described above, the fixed pattern noise is reduced, and further it is possible to realize high-speed reading. Furthermore, the S/N ratio of the signal can be improved as compared to the first embodiment.

Sixth Embodiment

FIG. **12** illustrates a configuration of an image pickup system according to the present embodiment. The image pickup system **800** includes, for example, an optical unit **810**, an image pickup element **100**, a video signal processing circuit unit **830**, a recording and communication unit **840**, a timing control circuit unit **850**, a system control unit **860**, and a reproduction and display unit **870**. An image pickup apparatus **820** includes the image pickup element **100** and the video signal processing circuit unit **830**. The photoelectric conversion apparatus according to any of the embodiments described above is used for the image pickup element **100**.

The optical unit **810** functioning as an optical system such as a lens focuses light from a subject onto a pixel array **03**, in which a plurality of pixels of the image pickup element **100** are two-dimensionally arranged, and forms an image of the subject. The image pickup element **100** outputs a signal in accordance with the light focused on the pixel array **03** at a timing based on a signal from the timing control circuit unit **850**. The signal output from the image pickup element **100** is input to the video signal processing circuit unit **830** functioning as a video signal processing unit, and the video signal processing circuit unit **830** performs signal processing in accordance with a method set by a program or the like. A signal obtained by the processing in the video signal processing circuit unit **830** is transmitted to the recording and communication unit **840** as image data. The recording and communication unit **840** transmits the signal for forming the image to the reproduction and display unit **870** and causes the reproduction and display unit **870** to reproduce and display a moving image or a still image. The recording and communication unit **840** further receives the signal from the video signal processing circuit unit **830** to perform communication with the system control unit **860** and also performs an operation for recording the signal for forming the image in a recording medium that is not illustrated.

The system control unit **860** is configured to control the operation of the image pickup system and controls drive of the optical unit **810**, the timing control circuit unit **850**, the recording and communication unit **840**, and the reproduction and display unit **870**. In addition, the system control unit **860** is provided, for example, with a storage device (not illustrated) such as a recording medium, and the program, or the like, to be used for controlling the operation of the image pickup system is recorded in this storage device. The system control unit **860** also supplies to the image pickup system a signal for switching a drive mode in accordance with, for example, an operation by a user. A few examples of drive modes include, changing a reading row or a row to be reset, changing a field angle accompanied by electronic zooming, and shifting the field angle based on an electronic image stabilizing function. The timing control circuit unit **850** controls driving timings of the image pickup element **100** and the video signal processing circuit unit **830** on the basis of the control performed by the system control unit **860**.

Others

The embodiments described above are intended as examples for carrying out the present invention and are not limited to these configurations.

For example, a voltage follower circuit or a source follower circuit can be applied as a specific configuration of the buffer unit **14**, and it is also possible to use the inverting amplifier as illustrated in FIG. **5**, an amplifier that can set an amplification factor exceeding 1, and further, an amplifier in which the amplitude factor is variable. By applying the amplifier having the configuration illustrated in FIG. **5** to the buffer unit **14**, it is possible to enhance the effect of suppressing the fixed pattern noise. This is because, since an output impedance of the differential amplifier OP is small and also the signal is held in the capacitor element whose one end is supplied with a fixed voltage, even if the influence of the change of the output of the comparison unit **18** propagates to the input capacitance Cin via the feedback capacitance Cf, this influence can be suppressed.

In addition, by preparing a line for supplying the fixed voltage to one node of the capacitor element included in the sample-and-hold unit **13** separately from a line for supplying the fixed voltage to a circuit arranged in the vicinity of the capacitor element, it is possible to reduce the influence when the output of the comparison unit **18** changes. Specifically, GND of the capacitor element and GND of the comparison unit **18** are supplied by mutually different lines.

The capacitor element included in the sample-and-hold unit **13** can also be formed in a different well region on a same semiconductor substrate where circuits arranged in the vicinity of the capacitor element are formed in a certain well region. Specifically, the capacitor element and the comparison unit **18** are formed in mutually different well regions. Accordingly, it is possible to reduce the influence when the output of the comparison unit **18** changes. In addition, the capacitor element included in the sample-and-hold unit **13** may be formed in a well region different from the region where the pixel array and the column amplifier are formed, on the same semiconductor substrate. With this configuration, contamination of noise from the pixel and the column amplifier can be suppressed during the period in which the capacitor element holds the signal.

Moreover, the count unit **10** may be configured such that the count unit **10** is individually provided to each of the plurality of comparison units **18**. In this case, each count unit also functions as the write memory **19** in FIG. **4**. Furthermore, in a case where the count units **10** are individually provided to the respective comparison units **18**, the count unit **10** may take a configuration where an up-count operation in which a count value increments and a down-count operation in which the count value decrements can be switched. According to this configuration, by switching the operations between the period NAD(n) and the period SAD(n), the digital signal in which the noise component is reduced can be held in the respective count units.

While the present invention has been described with reference to embodiments, it is to be understood that the invention is not limited to the disclosed embodiments. The scope of the following claims is to be accorded the broadest interpretation so as to encompass all such modifications and equivalent structures and functions.

This application claims the benefit of Japanese Patent Application No. 2013-160333, filed Aug. 1, 2013.

What is claimed is:

1. A photoelectric conversion apparatus comprising:

a pixel array in which a plurality of pixels are arranged in rows and columns; and

column signal processing units each provided in correspondence with one of the columns of the pixel array,

wherein each of the column signal processing units includes

a sample-and-hold unit configured to hold a signal output from the pixel,

a buffer unit configured to output the signal held in the sample-and-hold unit, and

an AD conversion unit including a comparison unit having a first terminal and a second terminal, the first terminal being connected to the buffer unit, the second terminal being configured to receive a reference signal whose level changes corresponding to elapsed time, wherein the comparison unit outputs a comparison signal indicating a result of comparing the level of the reference signal and a level of the signal buffered by the buffering unit,

wherein the buffer unit outputs the signal held by the sample-and-hold unit to the first terminal during a period that the level of the reference signal changes corresponding to the elapsed time, and

wherein the AD conversion unit converts the signal output from the buffer unit into a digital signal using the comparison signal.

2. The photoelectric conversion apparatus according to claim **1**,

wherein the sample-and-hold unit includes a capacitor element, one node of which is supplied with a fixed voltage.

3. The photoelectric conversion apparatus according to claim **2**,

wherein the comparison unit is configured to operate based on a fixed voltage and compare a reference signal and the signal output from the buffer unit, and

wherein the fixed voltage supplied to the capacitor element and the fixed voltage supplied to the comparison unit are supplied via mutually different lines.

4. The photoelectric conversion apparatus according to claim **2**, further comprising:

an amplifier configured to amplify the signal output from the pixel and supply the amplified signal to the sample-and-hold unit.

5. The photoelectric conversion apparatus according to claim **2**, further comprising:

a connecting portion that mutually connects the capacitor elements included in some of the column signal processing units among the plurality of column signal processing units.

6. The photoelectric conversion apparatus according to claim **1**,

wherein the sample-and-hold unit includes a plurality of capacitor elements.

7. The photoelectric conversion apparatus according to claim **1**,

wherein the buffer unit is an amplifier capable of setting an amplification factor exceeding 1.

8. The photoelectric conversion apparatus according to claim **1**,

wherein in parallel with an operation of outputting the signal from the pixel,

the AD conversion unit converts the signal buffered by the buffer unit into a digital signal.

9. The photoelectric conversion apparatus according to claim **1**, further comprising a count unit configured to generate a count signal,

wherein the AD conversion unit further comprises a memory unit configured to hold the count signal, and

wherein the memory unit holds the count signal as the digital signal converted from the signal buffered by the buffering unit, when a level of the signal output from the comparison unit changes.

10. A photoelectric conversion apparatus comprising:

a pixel array in which a plurality of pixels are arranged in a matrix; and

column signal processing units provided in correspondence with respective columns of the pixel array,

wherein the column signal processing unit includes

a sample-and-hold unit configured to hold a signal output from the pixel,

a buffer unit configured to buffer the signal held in the sample-and-hold unit, and

an AD conversion unit,

wherein the AD conversion unit converts the signal held by the sample-and-hold unit and buffered by the buffer unit into a digital signal,

wherein the sample-and-hold unit includes a capacitor element, one node of which is supplied with a fixed voltage,

wherein the AD conversion unit includes a comparison unit configured to compare a reference signal and the signal buffered by the buffer unit, and

wherein the capacitor element and the comparison unit are formed in different well regions of a same semiconductor substrate.

11. A photoelectric conversion apparatus comprising:

a pixel array in which a plurality of pixels are arranged in a matrix; and

column signal processing units provided in correspondence with respective columns of the pixel array,

wherein the column signal processing unit includes

a sample-and-hold unit configured to hold a signal output from the pixel,

a buffer unit configured to buffer the signal held in the sample-and-hold unit, and

an AD conversion unit,

wherein the AD conversion unit converts the signal held by the sample-and-hold unit and buffered by the buffer unit into a digital signal,

wherein the sample-and-hold unit includes a capacitor element, one node of which is supplied with a fixed voltage, and

wherein the capacitor element and the pixel array are formed in different well regions of a same semiconductor substrate.

12. A photoelectric conversion apparatus comprising:

a pixel array in which a plurality of pixels are arranged in a matrix;

column signal processing units provided in correspondence with respective columns of the pixel array; and

an amplifier configured to amplify the signal output from the pixel and supply the amplified signal to the sample-and-hold unit,

wherein the column signal processing unit includes

a sample-and-hold unit configured to hold a signal output from the pixel,

a buffer unit configured to buffer the signal held in the sample-and-hold unit, and

an AD conversion unit,

wherein the AD conversion unit converts the signal held by the sample-and-hold unit and buffered by the buffer unit into a digital signal,

wherein the sample-and-hold unit includes a capacitor element, one node of which is supplied with a fixed voltage, and

wherein the capacitor element and the amplifier are formed in different well regions of a same semiconductor substrate.

13. A photoelectric conversion apparatus comprising:

a pixel array in which a plurality of pixels are arranged in a matrix; and

column signal processing units provided in correspondence with respective columns of the pixel array,

wherein the column signal processing unit includes

a sample-and-hold unit configured to hold a signal output from the pixel,

a buffer unit configured to buffer the signal held in the sample-and-hold unit, and

an AD conversion unit,

wherein the AD conversion unit converts the signal held by the sample-and-hold unit and buffered by the buffer unit into a digital signal,

wherein the buffer unit includes a differential amplifier, an input capacitance, and a feedback capacitance, and

wherein an inversion input terminal of the differential amplifier is connected to the sample-and-hold unit via the input capacitance and connected to an output terminal of the differential amplifier via the feedback capacitance.

14. A photoelectric conversion apparatus comprising:

a pixel array in which a plurality of pixels are arranged in a matrix; and

column signal processing units provided in correspondence with respective columns of the pixel array,

wherein the column signal processing unit includes

a sample-and-hold unit configured to hold a signal output from the pixel,

a buffer unit configured to buffer the signal held in the sample-and-hold unit, and

an AD conversion unit,

wherein the AD conversion unit converts the signal held by the sample-and-hold unit and buffered by the buffer unit into a digital signal,

wherein the sample-and-hold unit includes a plurality of capacitor elements, and

wherein an operation, by the AD conversion unit, of converting a signal that is buffered by the buffer unit and held in one of the plurality of capacitor elements into a digital signal and an operation of causing another capacitor element among the plurality of capacitor elements to hold the signal output from the pixel are performed in parallel.

15. An image pickup system comprising:

a photoelectric conversion apparatus;

an optical system configured to form an image on the plurality of pixels; and

a video signal processing unit configured to process a signal output from the photoelectric conversion apparatus and generate image data,

wherein the photoelectric conversion apparatus comprises:

a pixel array in which a plurality of pixels are arranged in rows and columns; and

column signal processing units each provided in correspondence with one of the columns of the pixel array,

wherein each of the column signal processing units includes

a sample-and-hold unit configured to hold a signal output from the pixel,

a buffer unit configured to output the signal held in the sample-and-hold unit, and

an AD conversion unit including a comparison unit having a first terminal and a second terminal, the first terminal being connected to the buffer unit, the second terminal being configured to receive a reference signal whose level changes corresponding to elapsed time,

wherein the comparison unit outputs a comparison signal indicating a result of comparing the level of the reference signal and a level of the signal output from the buffering unit,

wherein the buffer unit outputs the signal held by the sample-and-hold unit to the first terminal during a period that the level of the reference signal changes corresponding to the elapsed time, and

wherein the AD conversion unit converts the signal output from the buffer unit into a digital signal using the comparison signal.

16. The image pickup system according to claim **15**,

wherein the image pickup system operates in a plurality of drive modes, and

wherein the buffer unit is an amplifier capable of setting a plurality of amplification factors in accordance with the drive modes.

17. A driving method for a photoelectric conversion apparatus, wherein the photoelectric conversion apparatus comprises:

a pixel array in which a plurality of pixels are arranged in rows and columns; and

column signal processing units each provided in correspondence with one of the columns of the pixel array,

wherein each of the column signal processing units includes:

a sample-and-hold unit,

a buffer unit configured to output the signal held in the sample-and-hold unit, and

an AD conversion unit including a comparison unit having a first terminal and a second terminal, the first terminal being connected to the buffer unit, the second terminal being configured to receive a reference signal whose level changes corresponding to elapsed time,

wherein the driving method comprises:

outputting a signal from the pixel,

holding, by the sample-and-hold unit, a signal output from the pixel

outputting the signal held in the sample-and-hold unit from the buffer unit during a period that the level of the reference signal changes corresponding to the elapsed time,

outputting a comparison signal, from the comparison unit, the comparison signal being a signal indicating a result of comparing the level of the reference signal and a level of the signal output from the buffering unit, and

converting, by the AD conversion unit, the signal buffered by the buffering unit, during a period when the buffer unit keeps buffering the signal held in the sample-and-hold unit, into a digital signal, using the comparison signal.

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